INTEGRATED CIRCUIT PACKAGING FOR IMPROVING EFFECTIVE CHIP-BONDING AREA

FIELD OF THE INVENTION

The present invention is relating to a process for making an integrated circuit package, particularly to a process for making an integrated circuit package for improving effective chip-bonding area using a B-stage film layer as a chip bond material.

BACKGROUND OF THE INVENTION

It is conventional technique to utilize B-stage compound to be a chip bond material, as disclosed in R.O.C. Taiwan Patent No. 455,970 entitled "multi-chip stacked package". The conventional B-stage compound is used for adhering two chips, it won't produce a stress between the two chips because the two chips have a same thermal coefficient. Also the B-stage compound is sealed inside the molding compound, so that the adhesive strength of the B-stage compound is not demanded severely.

When a B-stage compound is directly configured to adhere a chip to a substrate in integrated circuit package. As showed in Fig.1, at first a B-stage compound 13 is applied to the chip-attaching surface 11 of the substrate 10. Next, the back surface 23 of the chip 20 is compressed to the chip-attaching surface 11 of the substrate 10. The B-stage compound 13 is heated while compressed to become a fully cured C-stage film layer 13 that adheres the chip 20 to the substrate 10 during the chip-attaching step. The C-stage film layer 13 will not have any change in physical phase and any chemical reaction in the sequent process especially the molding step. Bonding wires 30 that are formed by wire-bonding technique connect the bonding pads 21 on the active surface 22 of the chip 20 with the pads 12 of the substrate 10, next a molding step is executed. However, the B-stage compound 13 is formed by printing or other liquid dispensing method so as not to have an attaching surface that is not flat completely, and cannot substantially adhere the chip 20 and the substrate 10 by the chip 20 attaching pressure.

A popcorn defect is easy to happen while executing reliability test such as moisture or burn-in test after packaging. Therefore, when the chip 20 is separated from the substrate 10 prior to molding in a test, it is evident that the C-stage film layer 13 on the substrate 10 has a bad effective chip-bonding area merely 50 % approximately against the entire chip-bonding region of the substrate 10, even smaller than 30 % (as showed in Fig.2). For that reason, the C-stage film layer 13 formed in chip-attaching step of the conventional process is not good enough to adhere the chip 20 and the substrate 10, also there are voids or gaps between the chip 20 and the substrate 10.

SUMMARY

The primary object of this invention is to provide a process for integrated circuit package for improving effective chip-bonding area. Passing through a chip-attaching step and an electrically connecting step, a chip bond material on a substrate is maintained as a B-stage film layer to bond a chip. Next a molding compound is formed on the substrate. Because the packing pressure for the molding compound is larger than the chip-attaching pressure, the B-stage film layer can further closely re-bond the chip for improving effective chip-bonding area in molding step.

The secondary object of this invention is to provide a packaging process using a B-stage film layer as a chip bond material. The B-stage film layer closely bonds the chip and the substrate. Because the B-stage film layer has a glass transition temperature (Tg) lower than chip-attaching temperature and has a thermosetting temperature lower than thermosetting temperature of the molding compound, the B-stage film layer can be closely compressed between the chip and the substrate to remove gaps or voids in the molding step.

In accordance with this invention, a packaging process for improving effective chip-bonding area comprises a plurality of steps as follows. The first step is to provide a substrate having a chip-attaching surface. Next, an A-stage liquid paste including thermosetting material and solvent is applied to the chip-attaching surface of the substrate.

Following, the substrate is heated in order to remove the solvent of the A-stage liquid paste, resulting that the A-stage liquid paste is transformed into a dry B-stage film layer without fully curing. A chip is attached to the chip-attaching surface of the substrate by adhesion of the B-stage film layer, but the B-stage film layer is not cured fully during the chip-attaching step. Then, the chip is electrically connected with the substrate having the B-stage film layer in the next step. Finally, a molding compound is formed by a molding step. The B-stage film layer is active during the molding step. The packing pressure for the molding compound is 1000psi~1500psi approximately that is larger than the chip-attaching pressure, so that the B-stage film layer can be closely compressed to re-bond the chip in order to improve the effective chip-bonding area. Preferably, the heating temperature in the molding step is 150℃~200℃ approximately higher than the fully curing temperature of the B-stage film layer so as to cure the B-stage film layer and the molding compound simultaneously.

DESCRIPTION OF THE DRAWINGS

Fig.1 is a cross sectional view of a substrate with an attached chip in a conventional integrated circuit packaging process.

Fig.2 is a photograph showing the effective chip-bonding area on the substrate in the conventional integrated circuit package.

Fig.3 is a flow chart of a packaging process for improving effective chip-bonding area in accordance with an embodiment of the present invention.

From Fig.4A to Fig.4F are cross sectional views of the substrate in the packaging process in accordance with the embodiment of the present invention.

Fig.5 is a cross sectional view of the integrated circuit package formed by the packaging process in accordance with the embodiment of the present invention.

Fig.6 is a cross sectional view of a substrate with an attached chip inside a mold in accordance with another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Referring to the drawings attached, the present invention will be described by means of the embodiments below.

According to an embodiment of the present invention, the packaging process for improving effective chip-bonding area comprises the steps as showed in Fig.3.

As showed in Fig.3 and Fig.4A, the first step 101 is to provide a substrate 110, the substrate 110 is a high density wiring substrate for integrated circuit package, such as BT printed circuit board, thin film wiring board or TAB tape. The substrate 110 has a chip-attaching surface 111, and a plurality of connect pads 112 (or fingers) are formed on the chip-attaching surface 111 for electrically connecting with the chip 130. But the location of the connect pads 112 is not limited, the connect pads 112 can be formed on the other surface of the substrate 110 in another instance. Advantageously, the other surface of the substrate 110 corresponding to the chip-attaching surface 111 is a surface-mounting surface 113 that is electrically connected with the chip-attaching surface 111 by vias.

Next, as showed in Fig.3 and Fig.4B, an applying step 102 is executed. An A-stage liquid paste 121 is formed on the chip-attaching surface 111 of the substrate 110 to be used as a chip bond material. The A-stage liquid paste 121 may be formed by a liquid coating method, such as printing, screen printing, stencil printing, spraying, spin coating or dipping method. In this embodiment, the A-stage liquid paste 121 is formed by screen printing technique without covering the connect pads 112. The A-stage liquid paste 121 includes multi-stage thermosetting resins such as polyimide, polyquinolin or benzocyclobutene and a solvent that may dissolve the foregoing thermosetting resins such as the mixed solvent of butyrolactone and cyclopentanone or 1,3,5-mesitylene. The glass transition temperature (Tg) of the A-stage liquid paste 121 should be between -40°C and 10°C.

Next, as showed in Fig.3 and Fig.4C, the heating step 103 is followed. The substrate 110 is heated to pre-curing the A-stage liquid paste 121. The solvent of the

A-stage liquid paste 121 is removed by heating, vacuum drying or ultraviolet rays curing so that the A-stage liquid paste 121 is transformed into a dry and adhesive B-stage film layer 122. The B-stage film layer 122 is thermoplastic and thermosetting property and generally is called "prepreg". The B-stage film layer 122 has a glass transition temperature (Tg) and a fully curing temperature. The B-stage film layer 122 is active to present various adhesive under various temperatures. The glass transition temperature (Tg) of the B-stage film layer 122 is between -10°C~100℃ approximately, preferably between 35℃～70℃. When the B-stage film layer 122 is under a temperature higher than the glass transition temperature (Tg) of the B-stage film layer 122 but lower than the fully curing temperature, the B-stage film layer 122 will becomes viscous and adhesive for attaching a chip. When the B-stage film layer 122 on the substrate 110 is under a temperature (about ＜35℃) lower than the glass transition temperature of the B-stage film layer 122, such as room temperature, the B-stage film layer 122 will become a dry film without adhesive for transporting and storing the substrate 110. Also, the fully cured temperature of the B-stage film layer 122 is about 175 ℃ close to the molding temperature in the molding step 106.

Then, as showed in Fig.3 and Fig.4D, the chip attaching step 104 is executed. A chip 130 is attached to the chip-attaching surface 111 of the substrate 110 under a raised temperature and a pressure, wherein the temperature for attaching the chip 130 should be higher than the glass transition temperature of the B-stage film layer 122. The B-stage film layer 122 becomes adhesive to bond the chip 130 with the substrate 110. In this embodiment, the back surface 133 of the chip 130 is bonded on the chip-attaching surface 111 of the substrate 110 by the B-stage film layer 122 according to correspondingly various packages. There are a plurality of the bonding pads 131 formed on the active surface 132 of the chip 130. It is important that the B-stage film layer 122 is maintained in a partially curing condition without fully curing the B-stage film layer 122 during the chip attaching step 104 and the electrically connecting step 105.

Thereafter, as showed in Fig.3 and Fig.4E, the electrically connecting step 105 is executed. The bonding pads 131 of the chip 130 are electrically connected with the connect pads 112 of the substrate 110 by the metal wires 140 that are formed by wire bonding. At this time, the B-stage film layer 122 is maintained without fully curing. Besides, tape automated bonding method (TAB) or other conventional techniques can be utilized for this electrical connection.

Finally, as showed in Fig.3 and Fig.4F, the molding step 106 is performed. The molding step 106 includes a filling sub-step and a packing sub-step for forming a molding compound 150 on the substrate 110 by molds 151,152. In the filling sub-step, the substrate 110 with the attached chip 130 and the B-stage film layer 122 is placed inside the mold cavity formed by an upper mold 151 and a lower mold 152. A molding compound 150 is filled into the mold cavity under a filling pressure until filling over 80 vol% of the mold cavity. The molding compound 150 includes thermosetting resin, curing agent, silicate filler, releasing wax and a few coloring agent. In the packing sub-step, the packing pressure higher that the filling pressure is applied to the molding compound 150 inside the mold cavity to remove voids in the molding compound 150 and the voids in the B-stage film layer 122. The packing pressure is about 1000psi ~1500psi approximately larger than the chip attaching pressure mentioned in the chip attaching step 104. After completing the chip attaching step 104 and the electrically connecting step 105, the B-stage film layer 122 is still in partially curing condition and can be deformed suitably. The B-stage film layer 122 is closely compressed under the high packing pressure for the molding compound 150, so that the voids and gaps inside the B-stage film layer 122 will be removed so as to improve effective chip-bonding area between the chip 130 and the substrate 110. Preferably, the heating temperature in the molding step 106 for curing the molding compound 150 is about 150℃~200℃ that matches the fully curing temperature of the molding compound 150, so that the B-stage film layer 122 and the molding compound 150 are cured simultaneously. After the molding step 106, the

B-stage film layer 122 is transformed into the C-stage film layer 123 (as showed in Fig.5) to be a stable fixed film layer. In this embodiment, a step follows the molding step 106 to plant a plurality of solder balls 160 on the surface-mounting surface 113 of the substrate 110, then the substrate 110 is diced and separated to construct a ball grid array (BGA) package with excellent reliability. The packaging process for improving effective chip-bonding area of the present invention is suitable for various packages, especially for chip scale package (CSP). The B-stage film layer 122 won't contaminate the connect pads 112 of the substrate 110, so that the connect pads 112 may be arranged to be closely near to the chip 130. Advantageously, after dicing the substrate 110 to form separate integrated circuit package, the chip-attaching surface 111 of the substrate 110 is not larger than 1.5 times the active surface 132 of the chip 130 in area so as to form a chip scale package (CSP).

Furthermore, the packaging process for improving effective chip-bonding area of the present invention can be utilized for other different packages. As showed in Fig.6, a substrate210 has a window 214, a B-stage film layer 222 is printed on a chip-attaching surface 211 of the substrate210 for bonding the active surface 232 of the chip 230. The B-stage film layer 222 has a coating region larger than the active surface 232 of the chip 230. Bonding pads 231 are formed on the active surface 232 of the chip 230, the active surface 232 of the chip 230 is attached to the chip-attaching surface 211 of the substrate 210 corresponding to the window 214 to expose from the bonding pads 231. The bonding pads 231 of the chip 230 are electrically connected with the connect pads 212 of the substrate 210 by the bonding wires 240. The B-stage film layer 222 is not fully cured during the chip attaching step 104 and the electrically connecting step 105. When the substrate 210 is sealed by an upper mold 251 and a lower mold 252, the packing pressure for the molding compound 250 also make the B-stage film layer 222 be closely compressed in order to improve effective chip-bonding area.

The above description of embodiments of this invention is intended to be illustrated

are not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the above disclosure.